



PATENT APPLICATION

Sheet 1 of 1

FORM PTO-1449

LIST OF PATENTS AND PUBLICATIONS FOR
APPLICANT'S INFORMATION DISCLOSURE
STATEMENT

(Use several sheets if necessary)

ATTY. DOCKET NO.

200208051-1

APPLICATION NO.

10/606,463

CONFIRMATION NO.

TBA

APPLICANT

Benjamin T. Percer, et al.

FILING DATE

06-26-2003

GROUP

TBA

REFERENCE DESIGNATION

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	PUBLICATION DATE	NAME	Pages, Columns, Lines Where Relevant Passages or Figures Appear
	1A				
	1B				
	1C				
	1D				
	1E				
	1F				
	1G				
	1H				
	1I				
	1J				
	1K				

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	PUBLICATION DATE	NAME OF PATENTEE OR APPLICANT	Pages/Columns/Lines Where Relevant Passages/Figures Appear	Check if Translation attached
M	1L	GB 1 219 001	01-13-1971			
M	1M	JP 5-2502	01-08-1993			
	1N					
	1O					
	1P					

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

AS	1Q	UK Search Report; Application No. GB0413501.8, November 5, 2004.				
K	1R	Tsukude, et al. "Highly Reliable Testing of ULSI Memories with On-Chip Voltage-Down Converters". IEEE Design & Test Of Computers. June 1993, pgs. 6-12.				
AS	1S	Berner, et al. "DC Voltage Margin Tester.. NB84092465. IBM Technical Disclosure Bulletin, Vol. 27, No. 4B, September 1984, pg 246.				
EXAMINER					DATE CONSIDERED	
					9/13/05	